REMARKS/ARGUMENTS

This Amendment is in response to the Office Action mailed November 6, 2006. Claims 1, 2, 5-8, and 11-17 were pending in the present application. This Amendment amends claims 1, 7, and 13, and cancels claims 15 and 17, leaving pending in the application claims 1, 2, 5-8, and 11-14 and 16. Reconsideration of the rejected claims is respectfully requested.

I. Rejection under 35 U.S.C. §103

(a) *Gray* and *Becker*

Claims 1, 2, 7-8, 13-14, and 16 are rejected under 35 U.S.C. 103(a) as being obvious over *Gray* (U.S. Pat. No. 6,816,923) in view of *Becker* (U.S. Pat. No. 6,950,884). Applicants respectfully submit that these references do not teach or suggest each element of these claims.

For example, Applicants' claim 1 as amended recites a memory controller, comprising:

> at least one bus interface, each bus interface being for connection to at least one respective device for receiving memory access requests;
> a memory interface, for connection to a memory device over a memory bus;
> a plurality of buffers in the memory interface; and
> control logic, for placing received memory access requests into a queue of memory access requests,
> wherein, in response to a received memory access request requiring multiple data bursts over the memory bus, each of said multiple data bursts is assigned by the control logic to a respective buffer of the plurality buffers in the memory interface, and data from each of said multiple data bursts is stored by the memory interface in the respective buffer, and
> wherein, **for a wrapping memory access request requiring multiple buffers, data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer by the control logic,** the beginning and end data for the memory access request being stored in the respective sub-buffers by the memory interface, **the storing of the beginning and end data in a single buffer avoiding the need for an additional data burst to obtain the end data,** and
> **wherein the control logic records a value of a pointer indicating a first sub-buffer of the single buffer storing the end data, such that the control logic is able to return to the indicated sub-buffer to retrieve the end data from the single buffer**

(*emphasis added*). Such limitations are neither taught nor suggested by these references, alone or in combination.

For example, *Gray* teaches a direct memory access (DMA) system including a DMA engine that includes a data reservoir having a number of memory buffers in order to consolidate memory buffers for the various devices into the DMA reservoir, the reservoir including portions

that correspond to different devices (col. 2, lines 34-47; col. 3, line 64-col. 4, line 18). The use of the consolidated memory reservoir provides the ability to centralize addressing and provide each device with data in a timely manner and with increased bandwidth (col. 2, lines 34-56). *Gray* consolidates memory into buffers in the data reservoir (shown in Fig. 3; also col. 2, lines 34-47; col. 4, lines 10-12).

As recognized in the Office Action, *Gray* does not teach or suggest a request requiring multiple data bursts and data required for a beginning and an end of the request being stored in a single buffer, for a wrapping memory access request requiring multiple buffers. Further, *Gray* does not teach or suggest control logic assigning different portions of a single request from a single device to different sub-buffers of the single buffer, and recording a pointer so that the control logic can come back to the single buffer in order to obtain the end portion of the data without requiring an additional data burst as recited in Applicants' claim 1 as amended. For at least these reasons, *Gray* cannot render obvious Applicants' claim 1 or the claims that depend therefrom.

Becker does not make up for the deficiencies in *Gray* with respect to Applicants' claim 1. *Becker* teaches a DMA device for transferring data between two processors (col. 1, lines 54-60; col. 4, lines 32-58). *Becker* teaches using "cyclic memories," wherein read and write access between the two processors takes place in rising or falling memory block order (col. 8, line 65-col. 9, line 6). For example, when the last block of one control information memory is reached, the first block is automatically written to as the next memory block (col. 8, line 65-col. 9, line 6). *Becker* does not, however, teach or suggest control logic assigning different portions of a single request from a single device to different sub-buffers of the single buffer, and recording a pointer so that the control logic can come back to the single buffer in order to obtain the end portion of the data without requiring an additional data burst as recited in Applicants' claim 1 as amended. For at least these reasons, *Becker* cannot render obvious Applicants' claim 1 or the claims that depend therefrom, either alone or in combination with *Gray*.

Even if for sake of argument there were motivation to combine *Gray* and *Becker*, which Applicants do not believe as set forth previously, combining *Becker's* circular buffer with *Gray's*

device-specific buffers would not result in a memory controller with control logic assigning different portions of a single request from a single device to different sub-buffers of the single buffer, and recording a pointer so that the control logic can come back to the single buffer in order to obtain the end portion of the data without requiring an additional data burst as recited in Applicants' claim 1 as amended.

For at least these reasons, the combination of *Gray* and *Becker* fails to teach or suggest each element of Applicants' claim 1 as amended, such that these references cannot render obvious Applicants' claim 1 or the claims that depend therefrom. Independent claims 7 and 13 recite limitations that similarly are not rendered obvious by these references for reasons including those cited above. Applicants therefore respectfully request that the rejection with respect to claims 1, 2, 7-8, 13-14, and 16 be withdrawn.

(b) *Gray, Becker,* and *Kuronuma*

Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being obvious over *Gray* and *Becker*, and further in view of *Kuronuma* (U.S. Pat. No. 6,859,848). Claims 5 and 11 depend from claims 1 and 7, respectively, which are not rendered obvious by *Gray* and *Becker* as discussed above. *Kuronuma* does not make up for the deficiencies in *Gray* and *Becker* with respect to these claims. *Kuronuma* teaches a memory control system for sequentially accessing an arbitrary address in an SDRAM circuit (col. 4, lines 22-25), and is cited as teaching sequential access to an SDRAM (OA page 13). *Kuronuma* does not, however, teach or suggest a memory controller with control logic assigning different portions of a single request from a single device to different sub-buffers of the single buffer, and recording a pointer so that the control logic can come back to the single buffer in order to obtain the end portion of the data without requiring an additional data burst. As such, *Kuronuma* cannot render obvious claims 1 and 7, or dependent claims 5 and 11, alone or in any combination with *Gray* and *Becker*. Applicants therefore respectfully request that the rejection with respect to claims 5 and 11 be withdrawn.

(c) *Gray*, *Becker*, and *Microsoft*

Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being obvious over *Gray* and *Becker*, and further in view of *Microsoft* ("Microsoft Computer Dictionary", 2002 p. 469). Claims 6 and 12 depend from claims 1 and 7, respectively, which are not rendered obvious by *Gray* and *Becker* as discussed above. *Microsoft* does not make up for the deficiencies in *Gray* and *Becker* with respect to these claims. *Microsoft* is cited as teaching SDRAM as a common type of RAM (OA page 14). *Microsoft* does not, however, teach or suggest a memory controller with control logic assigning different portions of a single request from a single device to different sub-buffers of the single buffer, and recording a pointer so that the control logic can come back to the single buffer in order to obtain the end portion of the data without requiring an additional data burst. As such, *Microsoft* cannot render obvious claims 1 and 7, or dependent claims 6 and 12, alone or in any combination with *Gray* and *Becker*. Applicants therefore respectfully request that the rejection with respect to claims 6 and 12 be withdrawn.

(d) *Gray*, *Becker*, and *Nguyen*

Claims 15 and 17 (please note typographical error in Office Action as also indicated in previous response) are rejected under 35 U.S.C. 103(a) as being obvious over *Gray* and *Becker*, and further in view of *Nguyen* (U.S. Pat. No. 5,335,326). Although Applicants do not agree with these rejections, it is respectfully submitted that claims 15 and 17 have been canceled from the present application such that the rejections are now moot.

II. Amendment to the Claims

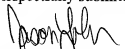
Unless otherwise specified or addressed in the remarks section, amendments to the claims are made for purposes of clarity, and are not intended to alter the scope of the claims or limit any equivalents thereof. The amendments are supported by the specification and do not add new matter.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 925-472-5000.

Respectfully submitted,



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